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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,237	01/14/2002	Yasuhiro Doumae	OKI.293	6211

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EXAMINER	
VESPERMAN, WILLIAM C	

ART UNIT	PAPER NUMBER
2813	3

DATE MAILED: 07/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/043,237	DOUMAE, YASUHIRO
	Examiner	Art Unit
	William C. Vesperman	2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 -17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6-8 and 12-14* is/are rejected.

7)☒ Claim(s) *3-5,9-11 and 15-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is in response to applicant's filing of January 14,

Claim Rejections - 35 USC § 1022.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless:
>
> b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 6, 7, 8, 12, 13, 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Pradeep et al. (US 5,866,448).

In regards to Claim 1, 2, 6, Pradeep et al. teaches (Figures 5 – 7, columns 4 – 5, lines 48 – 45) a method of manufacturing a field effect transistor having a semiconductor substrate with a main surface comprising: forming a conductive layer (26) on the main surface via a dielectric film (22); forming a gate electrode by etching the conductive layer (26) using a mask (40) formed thereon; forming a source region and a drain region (48) in the main surface; and forming pocket regions (24, 50) in the semiconductor substrate by implanting ion using the mask where the implanting process is carried out so as to head from an obliquely upward direction of the mask to the semiconductor substrate (20). Pradeep et al. teaches (Figure 7, colmn 5, lines 16 – 25) that the LDD profile (pocket) under the gate may be realized using large angle tilt (LAT) ion implantation.

In regards to Claims 7, 8, 13, 14 Pradeep et al. teaches ((Figures 5 – 7, columns 4 – 5, lines 48 – 45) a method of manufacturing a field effect transistor having a semiconductor substrate (20) with a main surface, comprising: forming a conductive layer on the main surface via a dielectric film (24); forming a mask (40) on the conductive layer (26); forming pocket regions (24, 50) in the semiconductor substrate (20) by implanting ion using the mask; forming a gate electrode by etching the conductive layer using the mask; forming a source region and a drain region (48) in the main surface using the gate electrode as a mask; and wherein the pocket regions (24, 50) underly the source and drain regions (48). In addition, Pradeep et al. teaches (Figure 7, column 5, lines 16 – 25) that the LDD profile or pockets under the gate electrode may be realized using large angle tilt (LAT) in combination a dopant with ion implantation.

Allowable Subject Matter

4. Claims 3, 4, 5, 9, 10, 11, 15, 16, 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter.

The prior art does not fairly teach or suggest a method of manufacturing a field effect transistor wherein, the mask has a width being less than a desired width to defined gate length, and the implanting process is carried out so as to head from an upward direction of the mask to the semiconductor substrate using the mask,

wherein a dielectric spacer is formed on a side wall of the mask after the implanting process and then the gate electrode is formed by etching the conductive layer using the mask with the dielectric spacer; and a method of manufacturing a field effect transistor wherein the gate electrode is formed so as to expand a width from a top surface to a bottom surface after the implanting process.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Han et al. (US 5,409,848) teaches an angled pocket implantation semiconductor device.

Tran et al.(US 2002/0068395 A1) teaches a double LDD device.

Wierzorek et al. (US 6,352,885) teaches a transistor having a increased gate insulation.

Dawson (US 6,087,706) teaches a compact transistor structure.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William C. Vesperman whose telephone number is 703-305-1939. The examiner can normally be reached on Mon. - Fri., 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 703-308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

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Art Unit 2813

June 26, 2003

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800